ABSTRACT OF THE DISCLOSURE

The present invention is a unified shader unit used in texture processing in graphics processing device. Unlike the conventional method of using one shader for texture coordinate shading and another for color shading, the present shader performs both operations. The unified shader uses the same precision for both texture coordinate and color shading, thus simplifying the complexity of programming for two separate conventional shaders with different levels of precision. Furthermore, the present invention uses enhanced scheduling logic to perform indirect texture and bump mapping in a single first-in, first-out (FIFO) memory structure and avoids the problems associated with large FIFOs with buffer registers found in conventional shaders. In one embodiment, a plurality of ALU - memory pairs are synchronized to form a plurality of pipelines to execution shading instructions. In another embodiment, a plurality of unified shaders are synchronized and connected together to processing shading operations concurrently.